OIPE JC71
JUL 13 2004
PATENT & TRADEMARK OFFICE

FIG. 1

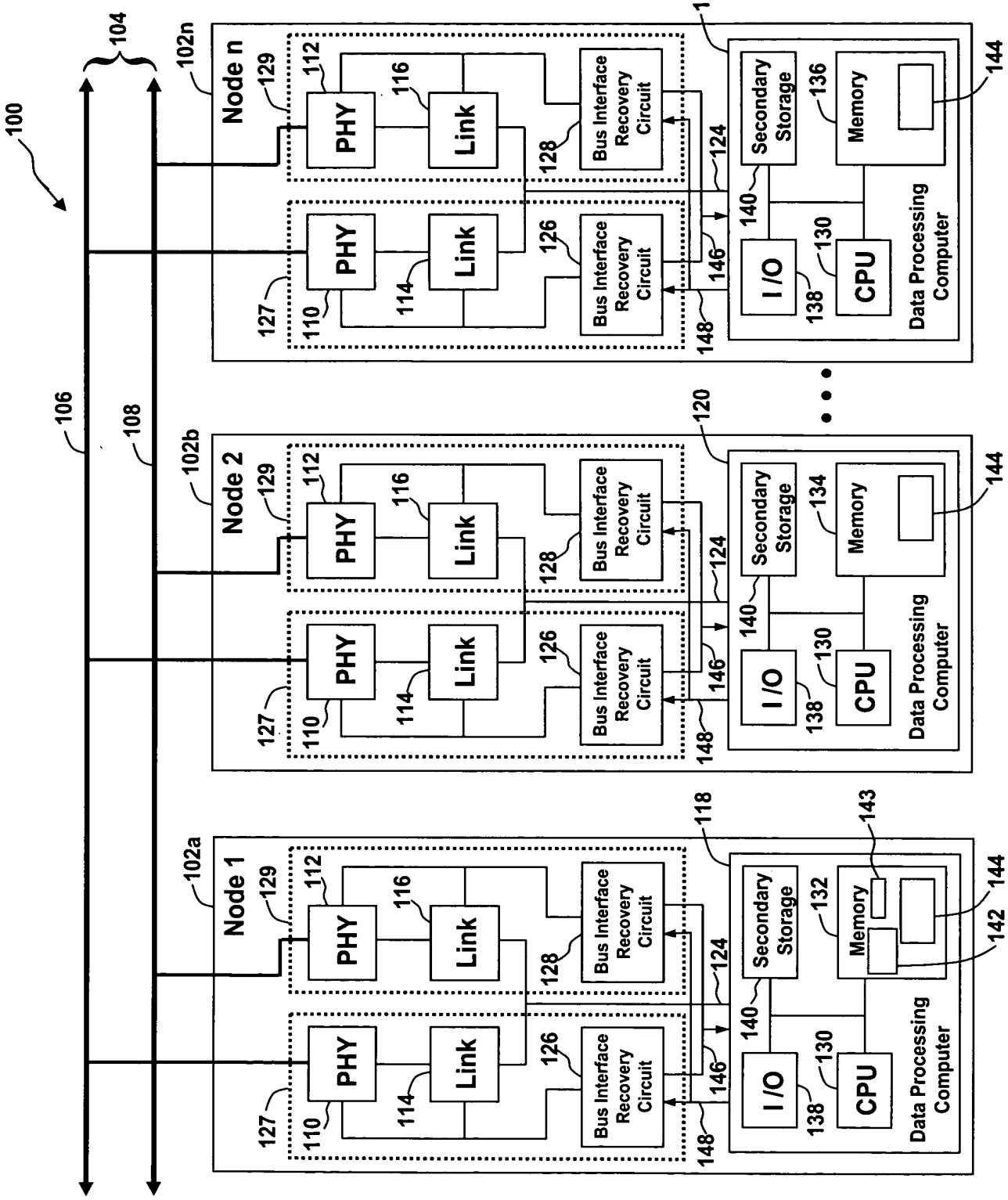


FIG. 2

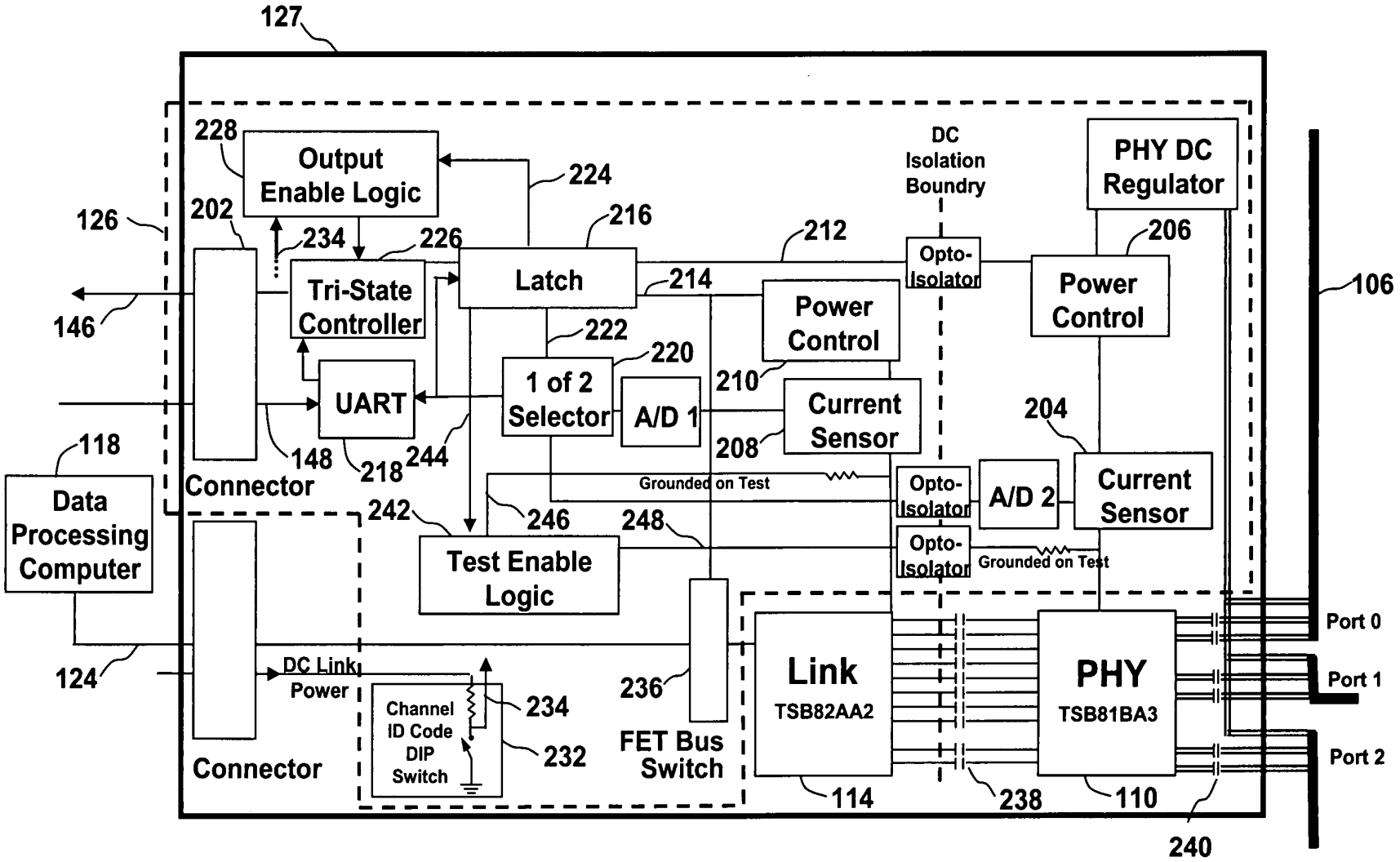

127
228
Output Enable Logic
224
DC Isolation Boundry
PHY DC Regulator
126
202
234
226
216
212
206
Tri-State Controller
Latch
Opto-Isolator
Power Control
106
146
214
222
220
210
Power Control
1 of 2 Selector
A/D 1
UART
Current Sensor
204
118
148
218
244
208
Connector
Grounded on Test
Opto-Isolator
A/D 2
Current Sensor
Data Processing Computer
242
246
248
Opto-Isolator
Grounded on Test
Test Enable Logic
Port 0
Port 1
Port 2
124
DC Link Power
Channel ID Code DIP Switch
234
232
236
Link TSB82AA2
PHY TSB81BA3
FET Bus Switch
Connector
114
238
110
240

FIG. 3

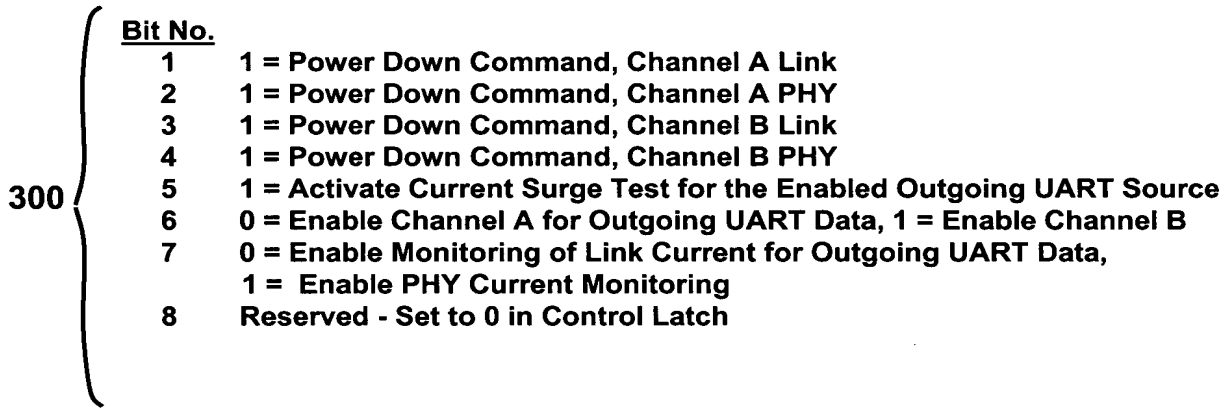

300
Bit No.
1 1 = Power Down Command, Channel A Link
2 1 = Power Down Command, Channel A PHY
3 1 = Power Down Command, Channel B Link
4 1 = Power Down Command, Channel B PHY
5 1 = Activate Current Surge Test for the Enabled Outgoing UART Source
6 0 = Enable Channel A for Outgoing UART Data, 1 = Enable Channel B
7 0 = Enable Monitoring of Link Current for Outgoing UART Data,
1 = Enable PHY Current Monitoring
8 Reserved - Set to 0 in Control Latch

FIG. 4

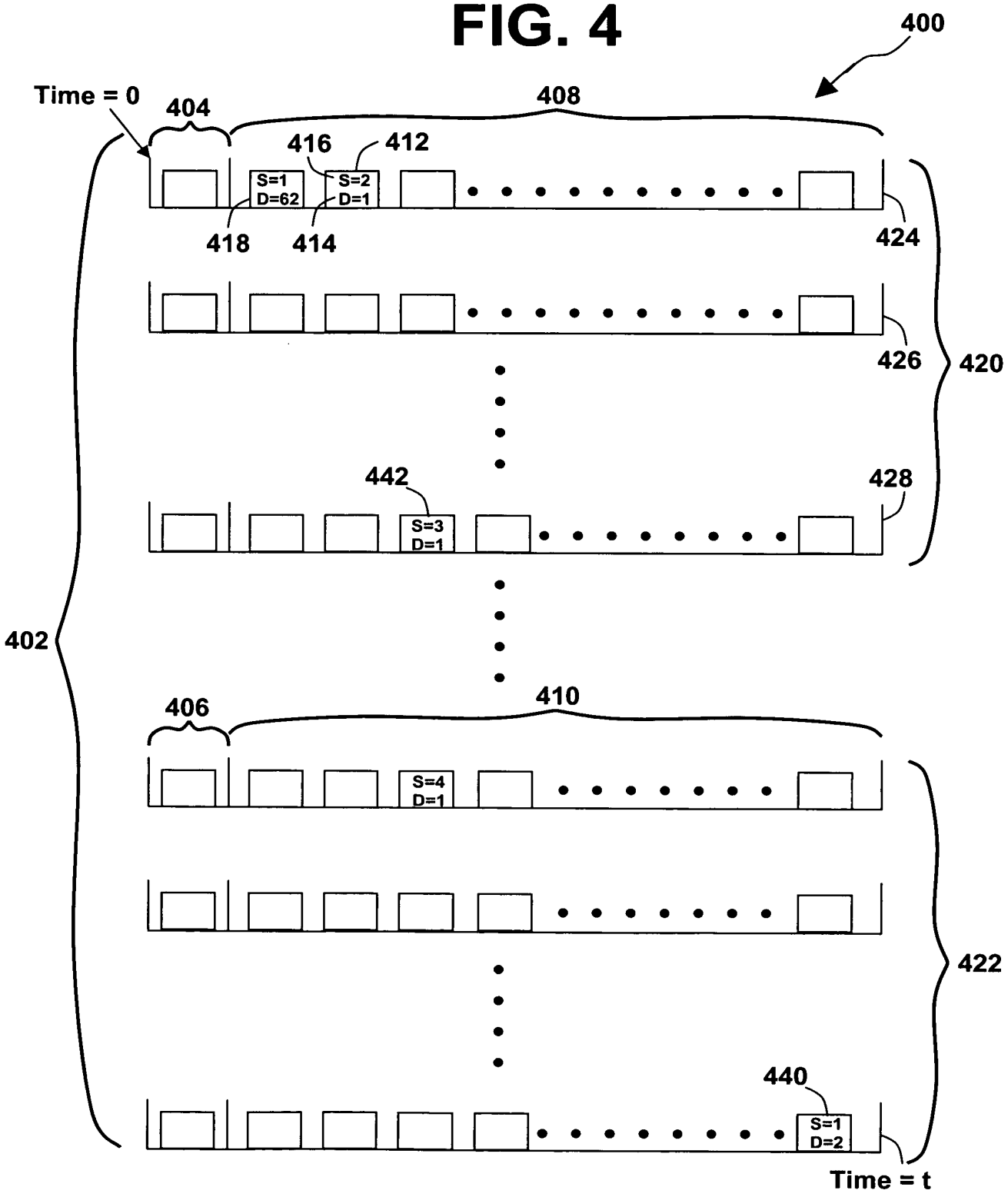

400
Time = 0
404
408
416
412
S=1
D=62
S=2
D=1
418
414
424
426
420
442
S=3
D=1
428
402
406
410
S=4
D=1
422
440
S=1
D=2
Time = t

FIG. 5

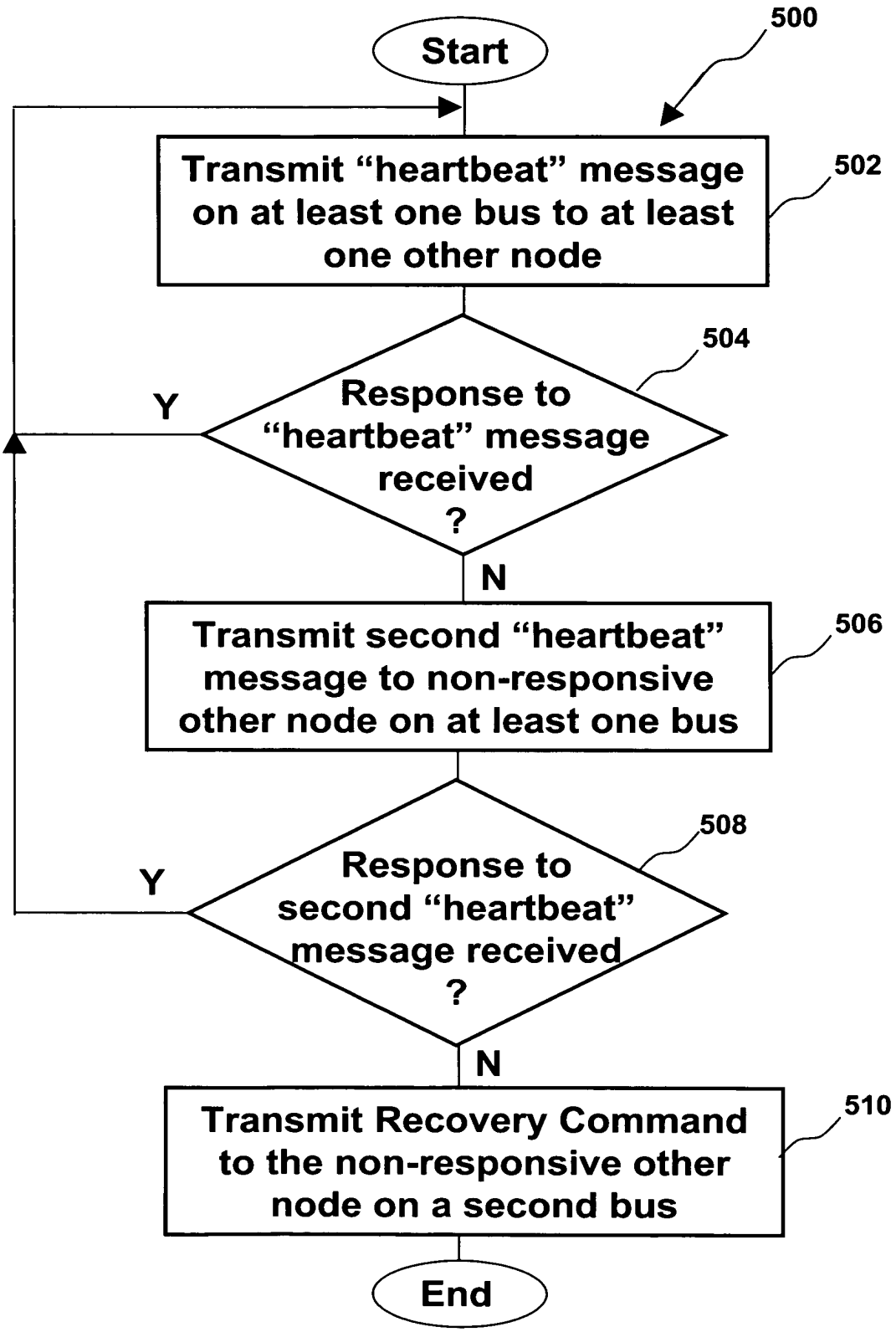

Start
500
Transmit "heartbeat" message on at least one bus to at least one other node
502
Response to "heartbeat" message received ?
504
Y
N
Transmit second "heartbeat" message to non-responsive other node on at least one bus
506
Response to second "heartbeat" message received ?
508
Y
N
Transmit Recovery Command to the non-responsive other node on a second bus
510
End

FIG. 6

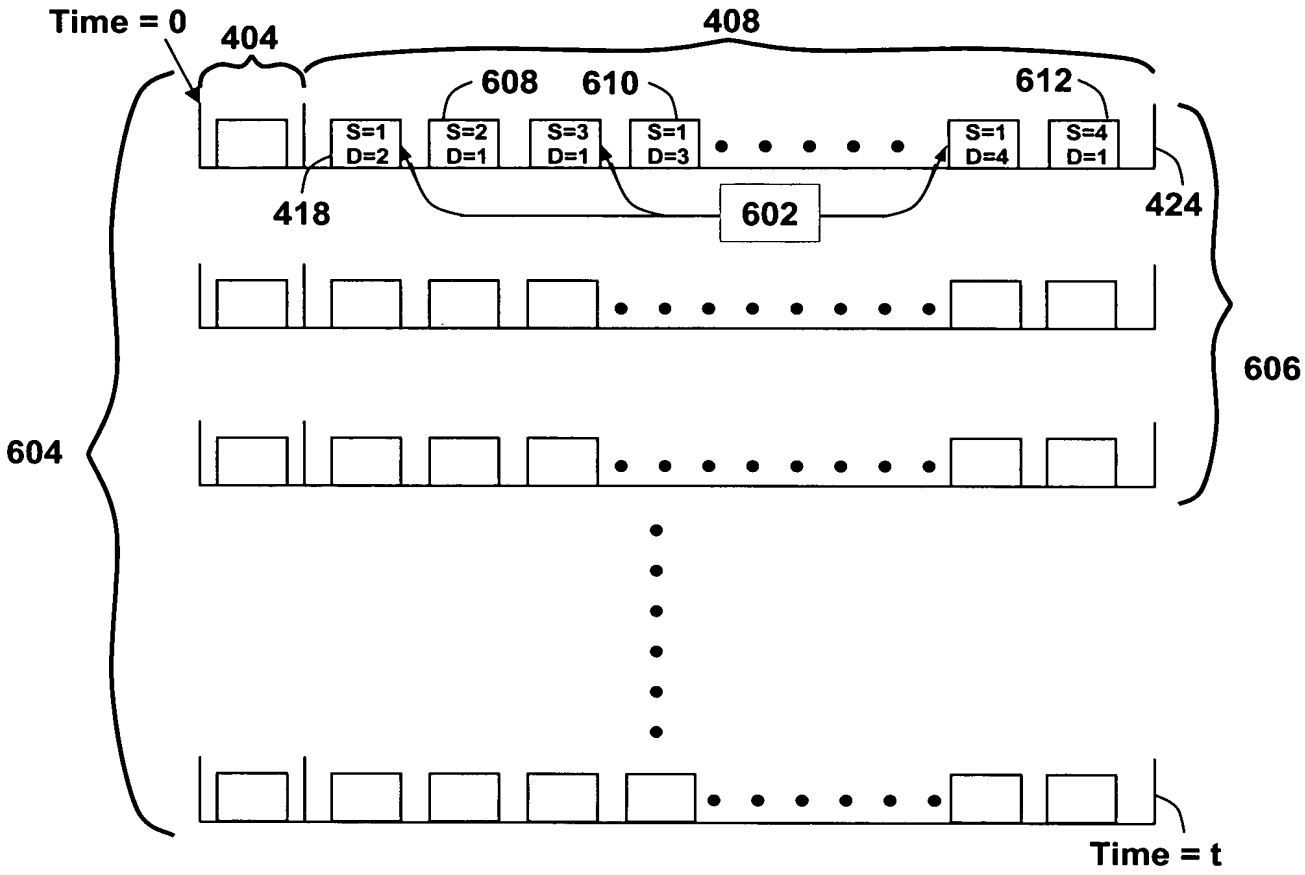

Time = 0
404
408
608
610
612
S=1
D=2
S=2
D=1
S=3
D=1
S=1
D=3
S=1
D=4
S=4
D=1
418
602
424
606
604
Time = t

FIG. 7

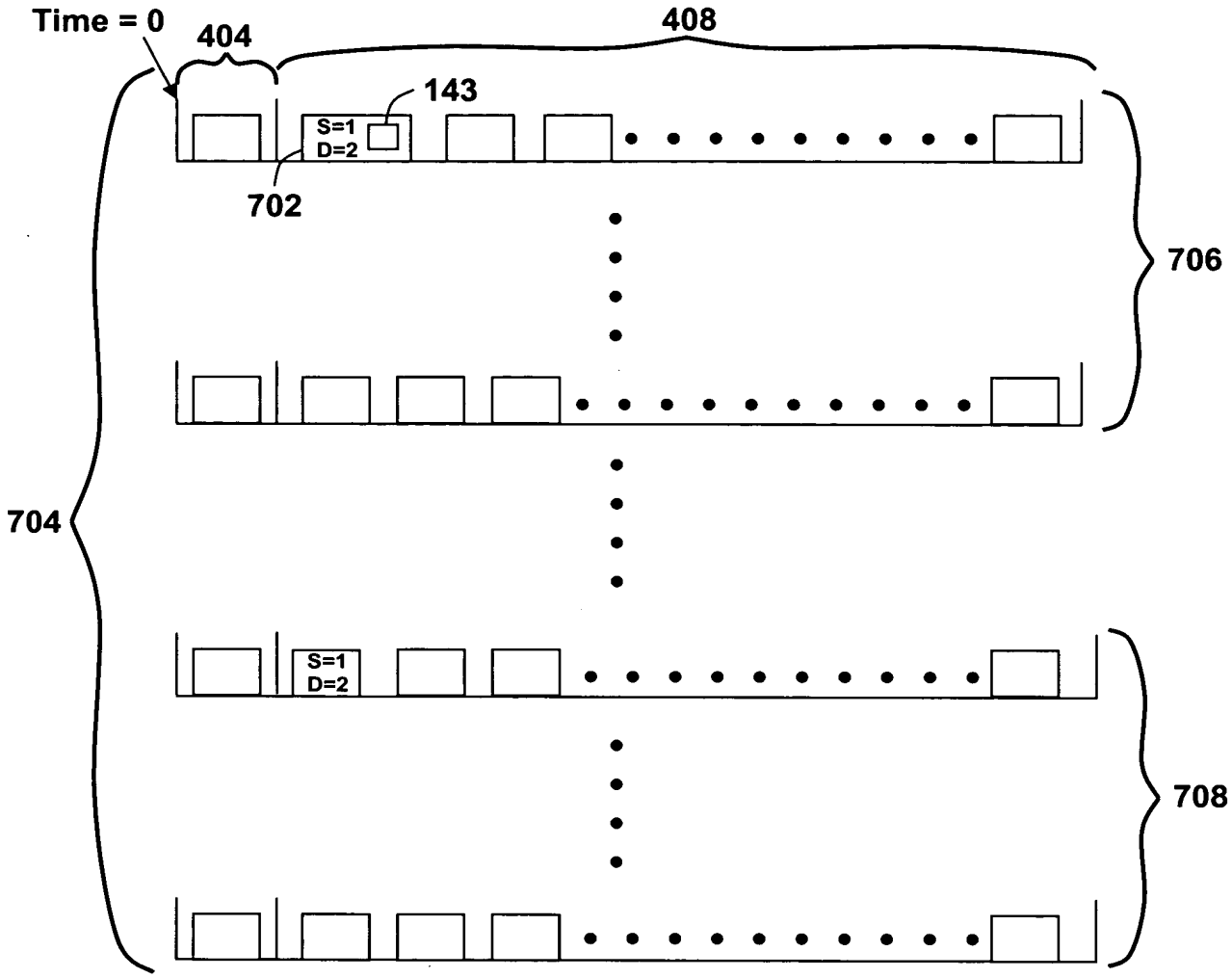


FIG. 8

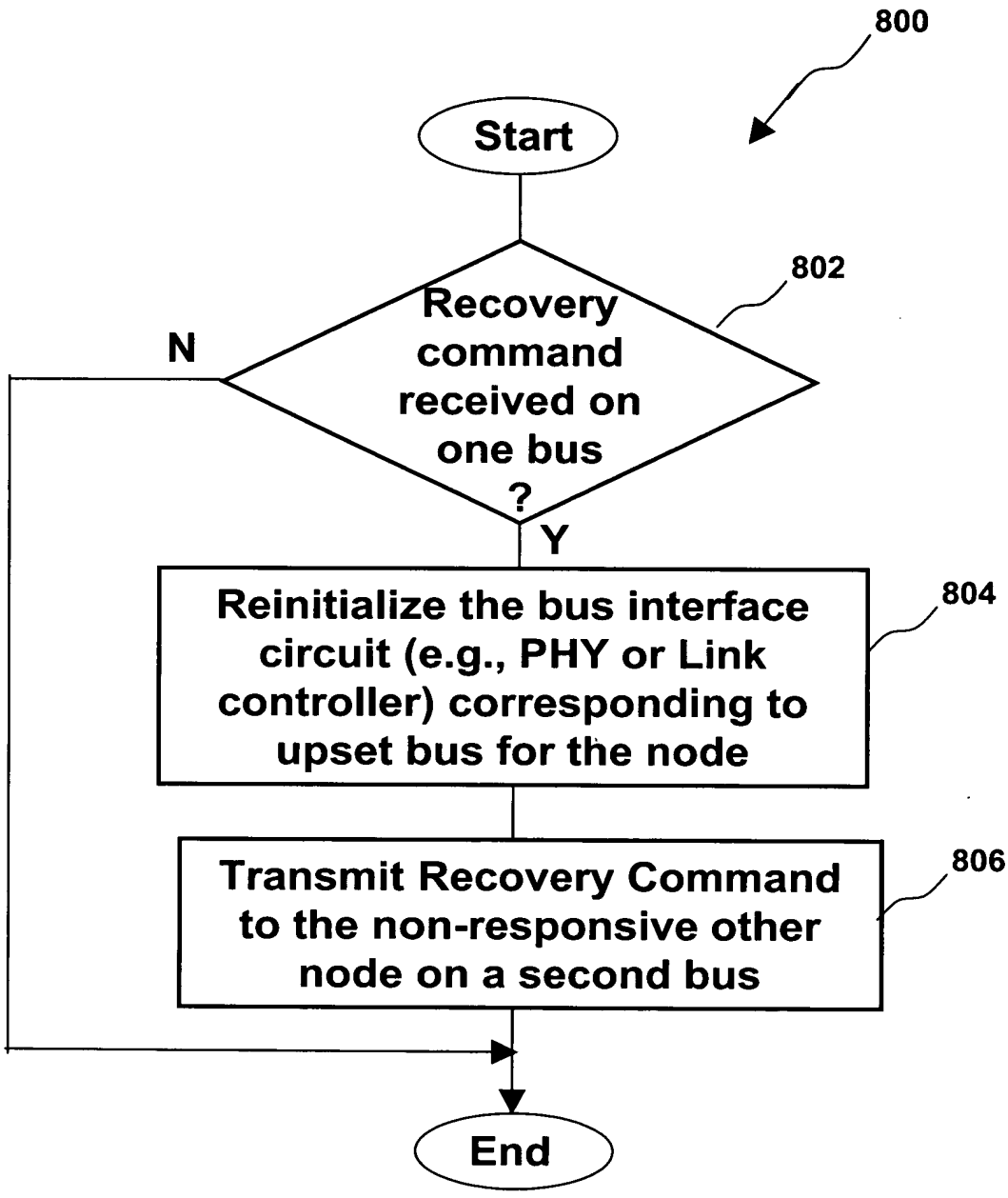

800
Start
802
Recovery command received on one bus ?
N
Y
Reinitialize the bus interface circuit (e.g., PHY or Link controller) corresponding to upset bus for the node
804
Transmit Recovery Command to the non-responsive other node on a second bus
806
End

FIG. 9

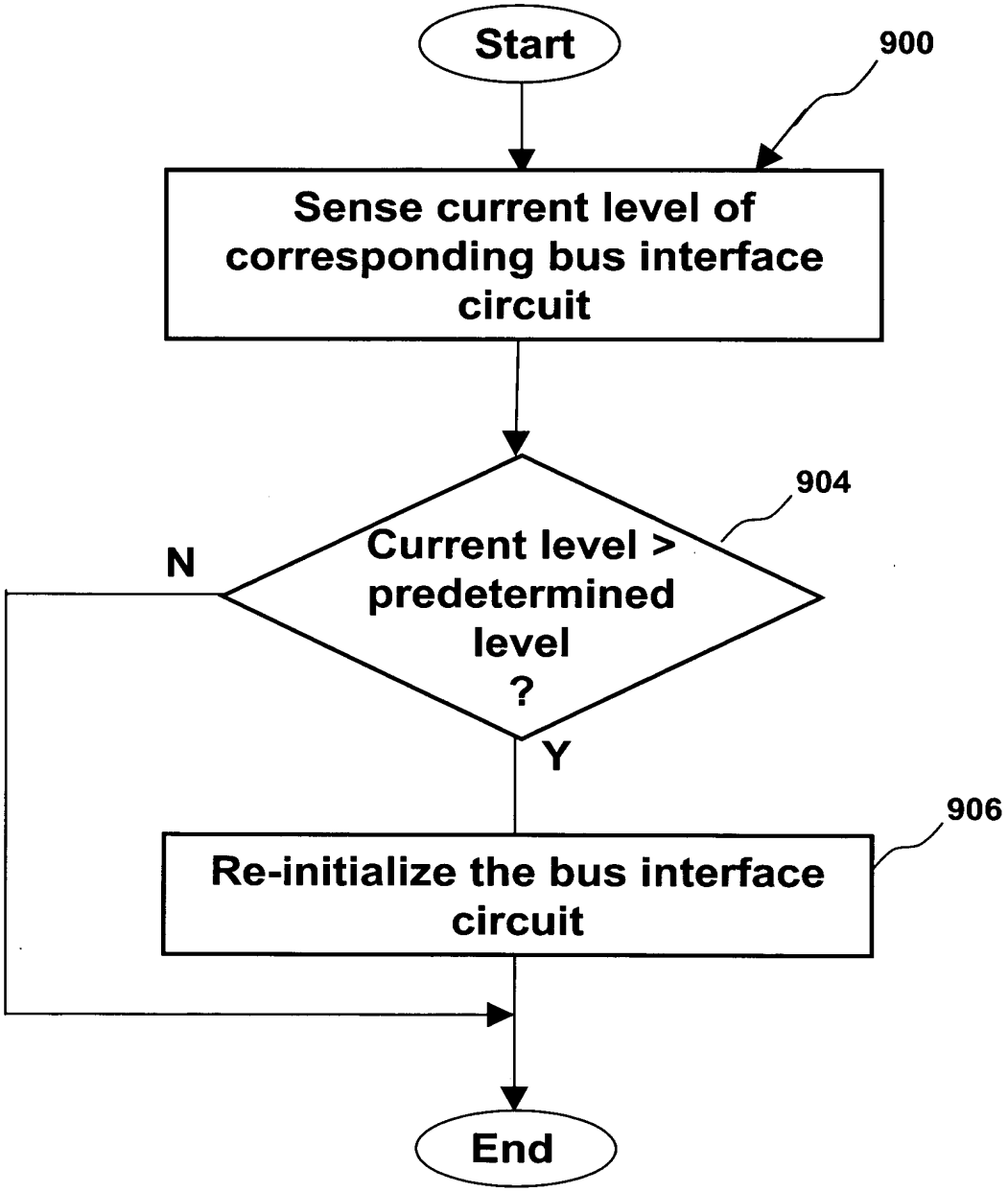
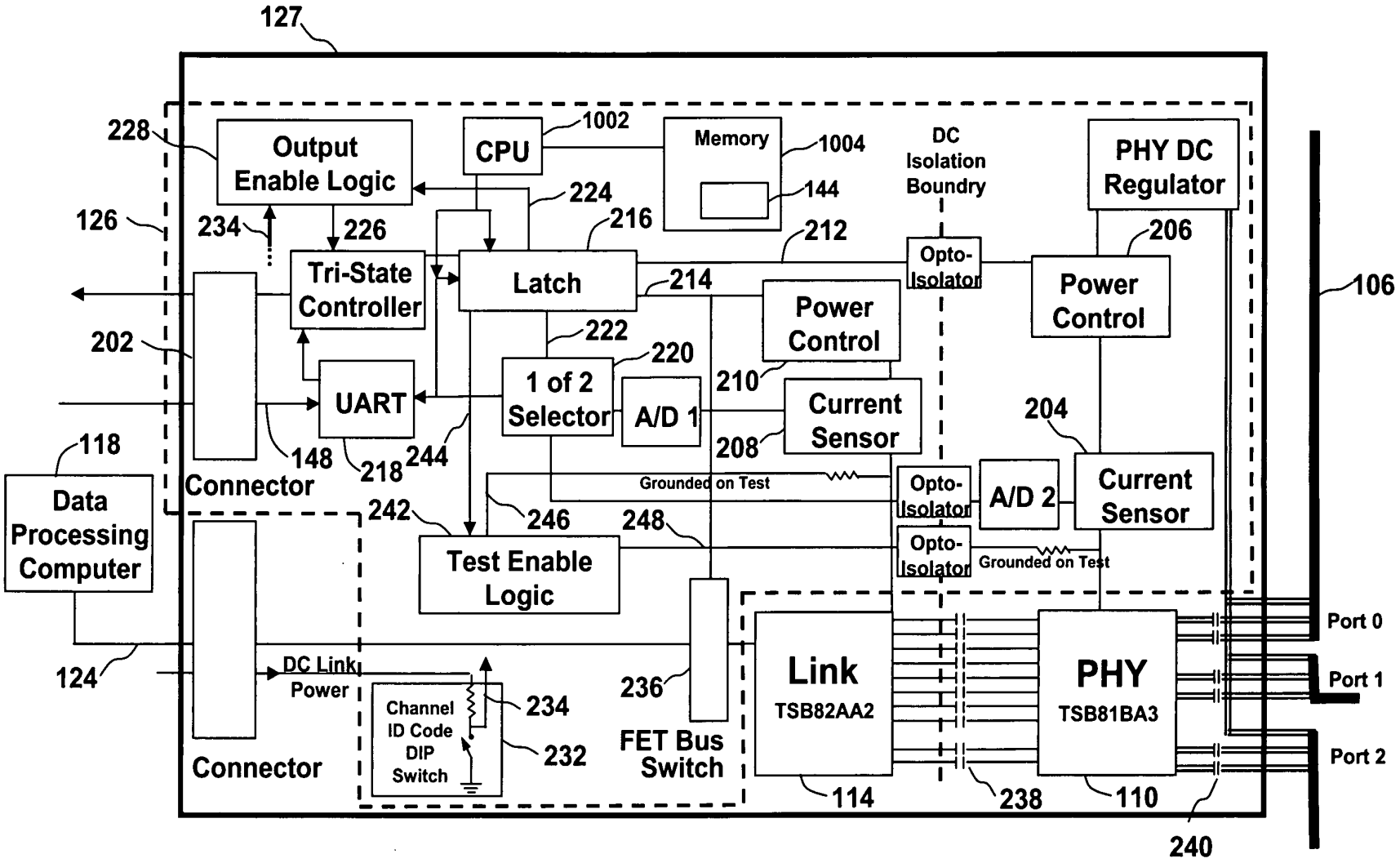

Start
900
Sense current level of corresponding bus interface circuit
904
Current level > predetermined level ?
N
Y
906
Re-initialize the bus interface circuit
End

FIG. 10


127
228
Output Enable Logic
CPU
1002
Memory
1004
144
DC Isolation Boundry
PHY DC Regulator
206
126
234
226
224
216
212
Tri-State Controller
Latch
214
Opto-Isolator
Power Control
106
202
222
220
UART
1 of 2 Selector
A/D 1
210
Power Control
Current Sensor
204
118
148
218
244
208
Connector
Grounded on Test
Opto-Isolator
A/D 2
Current Sensor
Data Processing Computer
242
246
248
Test Enable Logic
Opto-Isolator
Grounded on Test
Port 0
124
DC Link Power
Channel ID Code DIP Switch
234
232
236
FET Bus Switch
Link
TSB82AA2
PHY
TSB81BA3
Port 1
Port 2
Connector
114
238
110
240

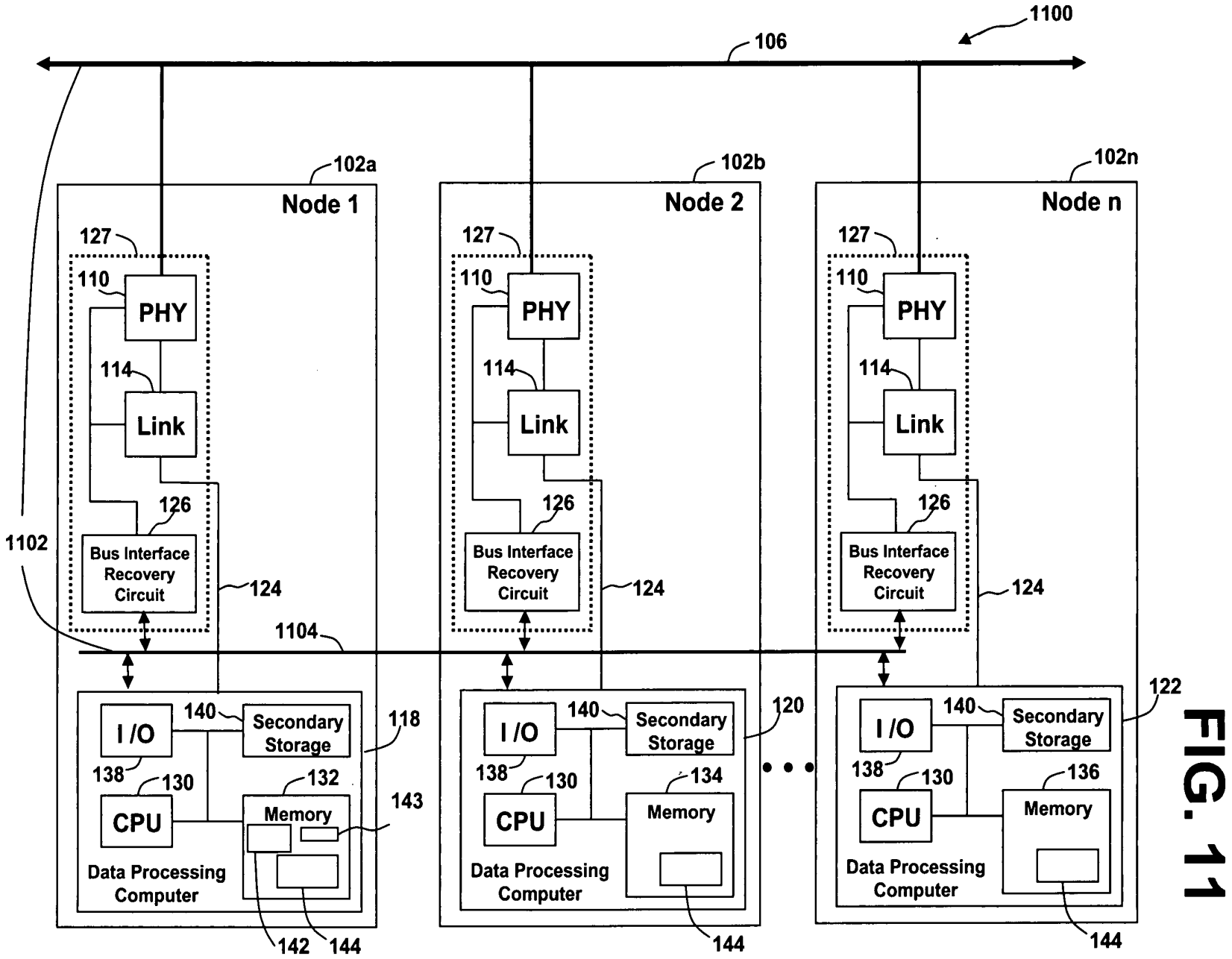

1100
106
102a
Node 1
102b
Node 2
102n
Node n
127
110
PHY
114
Link
126
Bus Interface Recovery Circuit
124
1102
1104
I/O
140
Secondary Storage
118
120
122
138
130
CPU
132
Memory
143
134
136
Data Processing Computer
142
144

FIG. 11